REMARKS

Present Status of the Application

Claims 1-14 are pending of which, claims 1-4 and 13 were rejected, claims 5-12 and 14 were previously withdrawn. Applicant has amended claims 1 and 3 to more clearly define the invention. No new matter adds by way of amendments made to claims or otherwise to the application. Entry of the amendments is requested.

Claim Rejection under 35 USC 102

1. The Office Action rejected claims 1 and 13 under 35 U.S.C. 102(b) as being anticipated by Quiley et al. (US-5,781,388, hereinafter Quiley).

Applicant respectfully traverses the rejection. Nevertheless, Applicant has amended claim 1 to more clearly define the invention.

The present invention is generally related to an ESD protection circuit. Particularly, claim 1, as amended, recites, among other things, "an anti-latch-up circuit, which comprises a fourth connection terminal, a fifth connection terminal, and a sixth connection terminal, respectively coupled to a voltage source, the ground voltage, and the third connection terminal of the SCR circuit, wherein the sixth connection terminal of the anti-latch-up circuit is directly connected to the third connection terminal of the SCR circuit, whereby an anti-latch-up signal is sent from the sixth connection terminal to the SCR circuit for preventing latching up of the SCR circuit during normal operation, wherein SCR circuit is directly triggered by an ESD event". In other words, the anti-latch up circuit, according to the present invention, is adapted for issuing an

anti-latch up signal to the SCR circuit for preventing latching up or triggering of the SCR circuit during the normal operation, however, the anti-latch up circuit does not generate any voltage to trigger the SCR circuit when an ESD event occurs, rather the ESD directly triggers the SCR circuit.

In this response, claim 1 has been further amended to specify that "the I/O pad is not directly connected to the voltage source and the anti-latch-up circuit".

In contrast, the capacitor 17 and the resistor 18 of Quiley, which the Examiner regards as a structure equivalent to an anti-latch up circuit, is in fact a voltage divider that function to generate an voltage to trigger the SCR circuit (please col. 4, lines 2-3). In other words, the SCR circuit is not directly triggered by the ESD event but rather triggered by the voltage generated by the voltage divider (17, 18).

Furthermore, as clearly shown in Fig. 1 of Quiley, the anti-latch-up circuit (17, 18, 21) of Quiley is directly connected to the I/O pad.

Accordingly, Applicants respectfully submit that Quiley cannot anticipate Claim 1. For at least the same reasons, claim 13, which directly depends from Claim 1, is not anticipated by Quiley either.

Reconsideration and withdrawal of the rejection is respectfully requested.

2. The Office Action rejected claims 1, 3, 4 and 13 under 35 USC 102(b) as being anticipated by Lin et al. (US-5,982,601, hereinafter Lin).

Applicant respectfully traverses the rejection.

Like Quiley as discussed above, Lin also substantially shows that the transient generator

(51), which the Examiner regards as a structure equivalent to an anti-latch-up circuit, is adapted to provide a voltage transition having a ramp rate faster than the ESD transient voltage's ramp rate in order to trigger the SCR circuit at an early stage of the ESD event (please see col. 2, line 66 to col. 3, line 6). In other words, the SCR of Lin is not directly triggered by the ESD event but rather triggered by the voltage generated by the transient generator (51).

Furthermore, the transient generator (51) is directly connected to the pad. In other words, the transient generator (51) is not connected to a voltage source as required by claim 1. While the amended claim 1 requires that the anti-latch-up circuit not be directly connected to the I/O pad.

Accordingly, Lin cannot anticipate Claim 1. For at least the same reasons, claims 3, 4, and 13, which directly depend from Claim 1, are not anticipated by Lin either.

Furthermore, claim 3 has been amended to recite "a diode is coupled to the second P+ doped region and the I/O pad at one end and coupled to the voltage source at the other end". Lin clearly does not teach or suggest such a feature.

Reconsideration and withdrawal of the rejection is respectfully requested.

Claim Rejection under 35 USC 103

3. The Office Action rejected claim 2 under 35 USC 103(a) as being unpatenble over Quiley in view of Ker et al. (US-5,754,380, hereinafter Ker).

Applicants respectfully disagree and would like to point out that even though the Examiner relied upon Ker a first diode and a second diode, still Ker cannot cure the specific deficiencies of Quiley as discussed above with respect to independent claim 1. Therefore, Claim 2, which directly depends from Claim 1 is also patentable over Quiley and Ker.

Reconsideration and withdrawal of the rejection is respectfully requested.

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-4 and 13 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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